IN THE SPECIFICATION

Please amend the paragraphs of the specification as follows:

On page 5, please replace the paragraph starting on line 19 with the following amended paragraph:

Another embodiment of the invention provides a method for processing a received signal in a wireless communications system. In accordance with the method, a transmitted signal is received, processed, and digitized to provide digitized samples at a particular sample rate. The digitized samples are then buffered in a first buffer, and segments of digitized samples [[and]] are retrieved from the first buffer and processed with a particular set of parameter values, some of which may be programmable. The processing is performed based on a processing clock having a frequency that is higher than the sample rate.

On page 8, please replace the paragraph starting on line 8 with the following amended paragraph:

FIG. 2 is a block diagram of a specific embodiment of a receiver unit 200 suitable for receiving and processing a modulated signal. Receiver unit 200 is a specific embodiment of receiver unit 130 in FIG. 1. The modulated signal is received by an antenna 212 and provided to a front-end unit 214. Within front-end unit 214, the received signal[[ ]] is amplified, filtered, frequency downconverted, and quadrature demodulated to provide baseband signals. The baseband signals are then digitized by one or more analog-to-digital converters (ADCs) with a sampling clock SCLK to generate inphase (I_{ADC}) and quadrature (Q_{ADC}) samples that are provided to a data interface circuit 222. Front-end unit 214 and ADCs 216 may be implemented within receiver 134 in FIG. 1.

On page 9, please replace the paragraph starting on line 22 with the following amended paragraph:

In some designs, a micro-controller 232 is provided to direct the operation of data processor 230. In such designs, micro-controller 232 receives directives or commands from controller 240 to perform particular tasks (e.g., perform correlation for one or all assigned fingers). Micro-controller 232 then directs operation of data processor 230 and other units (e.g., buffer 224, buffer/de-interleaver 234) to execute the tasks. Micro-controller 232 can reduce the

amount of supervision required by controller 240 and the interaction between controller 240 and other elements. Micro-controller 232 can thus free up controller 240 and ~~allows~~ allow it to support additional channels/users.

On page 16, please replace the paragraph starting on line 29 with the following amended paragraph:

For coherent demodulation, symbol demodulator and combiner 524 receives and coherently demodulates the decovered data symbols with the recovered pilot symbols to generate demodulated symbols that are stored to buffer/de-interleaver 234. For symbol combining, symbol demodulator and combiner 524 receives and combines demodulated symbols corresponding to various signal instances to generate recovered symbols that are stored back to buffer/de-interleaver 234. Symbol demodulator and combiner 524 can thus perform the functions performed by data correlator 410 and symbol ~~accumulator~~ combiner 450 in FIG. 4.

On page 30, please replace the paragraph starting on line 17 with the following amended paragraph:

A design and operation of a FHT element is described in further detail in U.S. Patent No. 5,561,618, entitled "METHODS AND APPARATUS FOR PERFORMING A FAST ~~HADANARD~~ HADAMARD TRANSFORM," issued October 1, 1996, assigned to the assignee of the present invention and incorporated herein by reference.

On page 34, please replace the paragraph starting on line 23 with the following amended paragraph:

The processing to be performed for search tasks, data processing tasks, signaling processing tasks, and other tasks are described in further detail in the following patents and patent applications, all of which are assigned to the assignee of the present invention and incorporated herein by reference in their entirety:

1) U.S. Patent Nos. 5,644,591 and 5,805,648, both entitled "METHOD AND APPARATUS FOR PERFORMING SEARCH ACQUISITION IN A CDMA COMMUNICATIONS SYSTEM[[";]],"
2) U.S. Patent Nos. 5,867,527 and 5,867,527, both entitled "METHOD OF SEARCHING FOR A BURSTY SIGNAL;"

3) U.S. Patent No. 5,764,687, entitled "MOBILE DEMODULATOR ARCHITECTURE FOR A SPREAD SPECTRUM MULTIPLE ACCESS COMMUNICATION SYSTEM;"
4) U.S. Patent No. 5,577,022, entitled "PILOT SIGNAL SEARCHING TECHNIQUE FOR A CELLULAR COMMUNICATIONS SYSTEM;"
5) U.S. Patent No. 5,654,979 entitled "CELL SITE DEMODULATION ARCHITECTURE FOR A SPREAD SPECTRUM MULTIPLE ACCESS COMMUNICATION SYSTEMS;"
6) U.S. Patent Application Serial No. 08/987,172, entitled "MULTI CHANNEL DEMODULATOR," filed December 9, 1997, now issued U.S. Patent No. 6,639,906, issued October 28, 2003 to Levin; and
7) U.S. Patent Application Serial No. 09/283,010, entitled "PROGRAMMABLE MATCHED FILTER SEARCHER," filed March 31, 1999, now issued U.S. Patent No. 6,363,108 issued March 26, 2002 to Agrawal et al.

On page 36, please replace the paragraph starting on line 4 with the following amended paragraph:

In the first clock cycle, the complex PN samples for eight chips are retrieved from buffer 224 and provided to latch 732 within correlator 732 (see FIG. 7A). In the second clock cycle, the data samples for the first two chips corresponding to time offsets of 0.0, 0.5, 1.0, and 1.5 are retrieved from buffer 224 and latched by latches 712a, 712b, 712c, and 712d, respectively. In the third clock cycles, the samples in latches 712 are re-latched by latches 714, and the data samples for the next two chips corresponding to time offsets of 2.0, 2.5, 3.0, and 3.5 are retrieved from buffer 224 and latched by latches 712a, 712b, 712c, and 712d, respectively. In the fourth clock cycle, the data samples for the first chip corresponding to time offsets of 0.0 and 0.5 are correlated by multipliers 720a and 720b, respectively, within correlator 522. In the fifth clock cycle, correlator 522 is ~~idled~~ idle. In the sixth clock cycle, the data samples for the second chip corresponding to time offsets of 1.0 and 1.5 are correlated by multipliers 720c and 720d, respectively. The processing performed for clock cycles seven through ten is similar to the processing performed for clock cycles three through six. The data processing further continues in similar manner until the next set of PN samples are needed and retrieved.